ANALOG DEVICES

AN-413
APPLICATION NOTE

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Evaluation Board for the AD7890, 12-Bit Serial, Data Acquisition System

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INTRODUCTION

This application note describes the evaluation board for the AD7890 12-bit serial data acquisition system. The AD7890 is an eight-channel 12-bit data acquisition system which operates from a single +5 V supply and contains an input multiplexer, on-chip track-and-hold amplifier, high speed 12-bit ADC, 2.5 V reference and a high speed serial interface. The AD7890 accepts an analog input range of ±10 V, 0 to 4.096 V or 0 V to +2.5 V depending on the version of the part being used. The part contains an on-chip control register accessible via the serial port and allows control of channel selection, conversion start, and power down of the part. This flexible serial interface allows the AD7890 to connect directly to digital signal processors (ADSP-2101, TMS320C25, etc.) and microcontrollers (8XC51, 68HC11, etc.). Full data on the AD7890 is available in the AD7890 data sheet available from Analog Devices and should be consulted in conjunction with this application note when using the evaluation board.

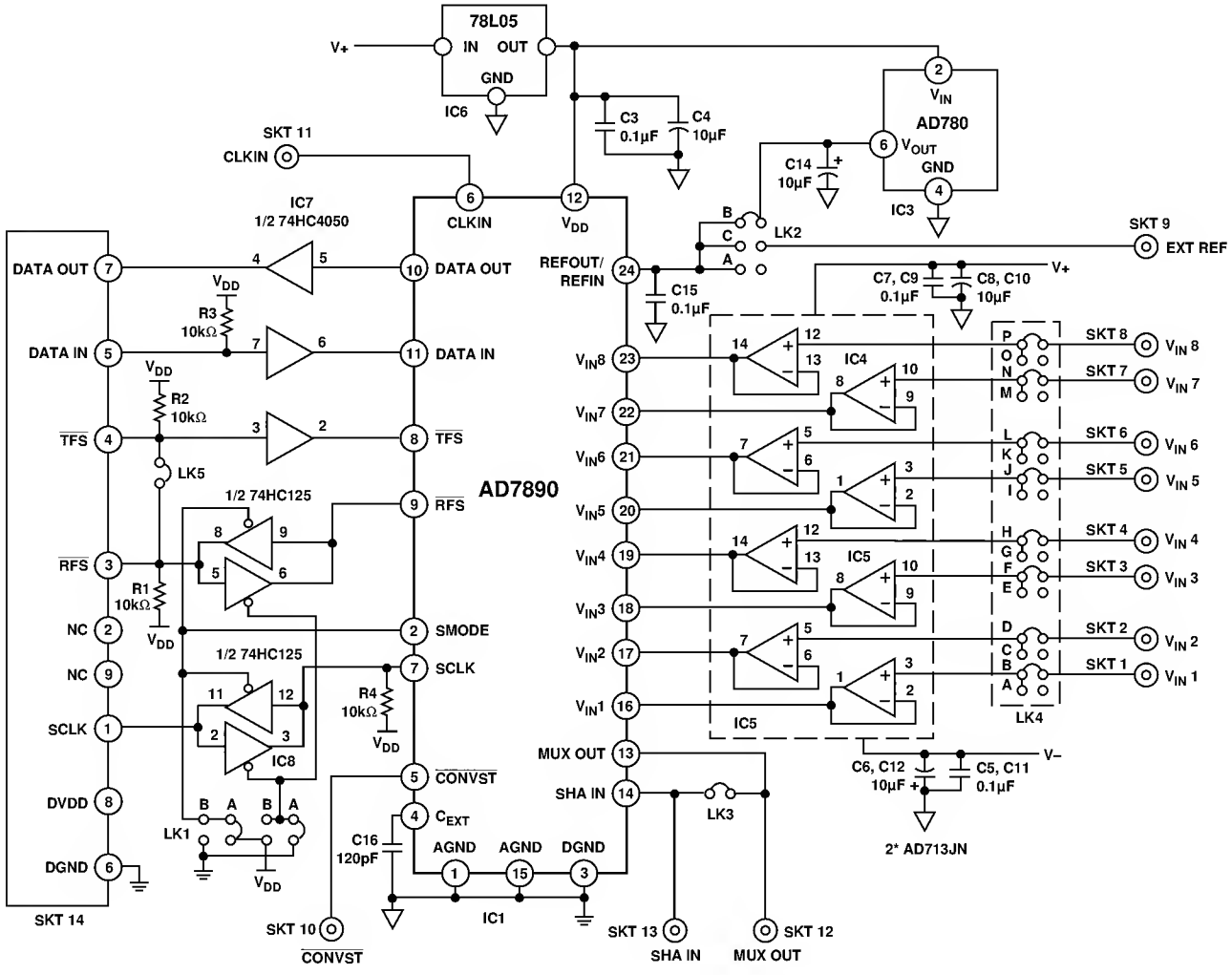

Figure 1. Evaluation Board Circuit Diagram

Onboard components include an AD780, a pin programmable +2.5 V or +3 V ultrahigh precision bandgap reference, bus buffers for the serial data lines and input buffer amplifiers to buffer the eight analog inputs. Interfacing to this board is through a 9-way D-type connector. External sockets are provided for the conversion start input, analog inputs, clk in, mux out, sha in and external reference input options.

OPERATING THE AD7893 EVALUATION BOARD

Power Supplies

This evaluation board has three analog power supply inputs: AV_{DD}, AGND and V_{SS}. These supplies are +15 V, 0 V and –15 V respectively and are used to power the onboard AD713 buffer amplifiers. The +15 V supply is used in conjunction with the LM78L05, a 5 V linear regulator, to provide the V_{DD} for the AD7890 and the V_{IN} for the AD780 voltage reference. There are two digital power supply inputs, DV_{DD} and DGND, that are used to power the digital logic on the board. These supplies can be provided through the D-type connector or through the connection pins labelled on the board.

All supplies are decoupled to ground with 10 μF tantalum and 0.1 μF ceramic disc capacitors. The AV_{DD} and V_{SS} supplies are decoupled to the AGND plane while the DV_{DD} supply is decoupled to the DGND plane.

The evaluation board uses extensive ground planing to minimize any high frequency noise interference from the onboard clocks or any other sources. Once again, the ground planing for the analog section is kept separate from that for the digital section and they are joined only at the AD7890 AGND and DGND pins.

Shorting Plug Options

There are five shorting plug options that must be set before using the evaluation board. These are outlined below:

LK1 This is a double link used to configure the bidirectional buffer on the SCLK and $\overline{RFS}$ inputs to the AD7890. The position of this link also controls the SMODE pin on the AD7890 configuring the part for self-clocking or external clocking mode of operation. In the external clocking mode both links of LK1 must be in Position A, setting the SMODE pin on the AD7890 to a logic high and routing the $\overline{RFS}$ and SCLK signals from the 9-way D-type connector to the AD7890. In the self-clocking mode both links on LK1 must be in Position B, configuring the SMODE pin on the AD7890 to a logic low and routing the $\overline{RFS}$ and SCLK output signals from the AD7890 to the 9-way D-type connector.

LK2 This option is used to select the reference source for the AD7890 REFIN/REFOUT pin.

With this link in Position A, the on-chip 2.5 V reference is used as the reference for the AD7890. The output impedance of this reference is 2 kΩ allowing this reference to be overdriven when using an external 2.5 V reference. In Position B, the AD780 2.5 V reference is selected as the reference for the AD7890. In Position C the reference for the part is provided from the external socket SKT9.

LK3 This link, when in place, connects the MUX OUT to the SHA IN. When this link is removed, the output of the multiplexer appears at the MUX OUT pin and also at MUX OUT (SKT12), and thus the user can insert an antialiasing filter or signal conditioning between the multiplexer and the ADC. The output range from the MUX OUT is 0 V to 2.5 V and the output impedance is 3.5 kΩ. The SHA IN is the input to the on-chip track and hold and is a high impedance input and accepts signals in the range of 0 V to 2.5 V. The SHA IN pin can be driven directly from SKT13 with LK3 removed.

LK4 This provides two options on each of the analog input channels. Option one selects the analog input for each channel from the external socket. The second option facilitates the use of the grid for signal conditioning and the signal can be linked to the V_{IN}. The following table describes the options associated with LK4.

Table I. Options Associated with LK4

Option	Function
A	Grid to V_{IN1} via buffer amplifier
B	SKT1 to V_{IN1} via buffer amplifier
C	Grid to V_{IN2} via buffer amplifier
D	SKT2 to V_{IN2} via buffer amplifier
E	Grid to V_{IN3} via buffer amplifier
F	SKT3 to V_{IN3} via buffer amplifier
G	Grid to V_{IN4} via buffer amplifier
H	SKT4 to V_{IN4} via buffer amplifier
I	Grid to V_{IN5} via buffer amplifier
J	SKT5 to V_{IN5} via buffer amplifier
K	Grid to V_{IN6} via buffer amplifier
L	SKT6 to V_{IN6} via buffer amplifier
M	Grid to V_{IN7} via buffer amplifier
N	SKT7 to V_{IN7} via buffer amplifier
O	Grid to V_{IN8} via buffer amplifier
P	SKT8 to V_{IN8} via buffer amplifier

LK5 This link in place connects $\overline{RFS}$ and $\overline{TFS}$ together and is useful in applications which require that data be transmitted and received at the same time.

EVALUATION BOARD INTERFACING

Interfacing to the evaluation board is via a 9-way D-Type connector, SKT14. The pinout for this connector is shown in Figure 2, and its pin designations are given in Table II.

SKT14 PIN DESCRIPTION

SCLK — Serial Clock Input/Output. In the external clocking mode (LK1 in Position A) an external serial clock is applied through this input to load data to the control register and to access data from the output register. In the self-clocking mode (LK1 in Position B) the internal serial clock is used to load data to the control register and to access data from the data register. This clock appears at the SCLK pin. The internal serial clock is derived from the master clock. This serial clock is buffered using a 74HC125 three-state buffer on the evaluation board and LK1 determines the direction of this bidirectional buffer depending on the mode of operation.

$\overline{RFS}$ — Receive Frame Sync. This can be an input or output depending on the mode of operation. In external clocking mode this pin is used to provide an active low framing pulse to access data from the data register. In the self-clocking mode an active low framing pulse which is internally generated by the part appears at this pin. This $\overline{RFS}$ signal is buffered on the board using a 74HC125 three-state buffer configured for bidirectional operation using LK1.

$\overline{TFS}$ — Transmit Frame Sync. This buffered input controls the AD7890 $\overline{TFS}$ input, and serial data is expected after the falling edge of this signal. There is a 10 kΩ pull-up resistor on this line to pull it to its inactive state if left unconnected.

DATA IN — This buffered input pin is used to provide the serial data to be loaded to the control register of the AD7890.

DGND — Digital Ground. This line is connected to the digital ground plane on the evaluation board. It allows the user to provide the digital supply via the connector along with the other digital signals.

DATAOUT — Serial Data Output. Serial data from the part is obtained at this output. This data is buffered by 74HC4050 hex buffer before arriving at the DATAOUT pin of the connector. The serial data is clocked out by the rising edge of SCLK and is valid on the falling of SCLK.

DV_{DD} — Digital +5 V Supply. This line is connected to the DV_{DD} supply line on the evaluation board. It allows the user to provide the digital supply via the connector along with the other digital signals.

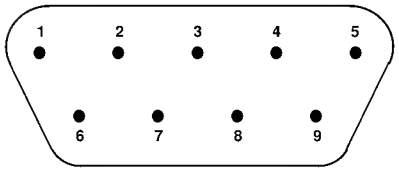

Figure 2. Pin Configuration for SKT14, D-Type Connector

Table II. SKT14 Pin Functions

Pin No.	Mnemonic
1	SCLK
2	N/C
3	$\overline{RFS}$
4	$\overline{TFS}$
5	DATA IN
6	DGND
7	DATAOUT
8	DV_{DD}
9	N/C

SOCKETS

There are fourteen sockets relevant to the operation of the AD7890 on this evaluation board. The functions of these sockets are outlined in Table III.

Table III. Socket Functions

Socket	Function
SKT1–SKT8	Subminiature BNC Sockets for the Eight Analog Input Channels
SKT9	Subminiature BNC Socket for External Reference
SKT10	Subminiature BNC Socket for CONVST Input
SKT11	Subminiature BNC Socket for Master Clock Input
SKT12	Subminiature BNC Socket for MUX OUT. The output of the on-chip multiplexer appears at this pin.
SKT13	Subminiature BNC Socket for the SHA IN Pin. An input to the on-chip track/hold can be applied to this socket.
SKT14	9-Way D-Type Connector

SET-UP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. Figure 5 shows the silkscreen layout of the board in order to ease setup. The following are the required link positions for the two modes of operation.

External Clocking Mode

LK1 Both links in Position A configuring both SCLK and $\overline{RFS}$ as inputs.

LK2 This link selects the reference input and can be placed in any of the 3 positions. A–internal reference, B–AD780, C–external reference from SKT9.

LK3 This should be in place connecting MUX OUT to SHA IN.

LK4 There should be a link inserted in each of the following positions to connect the analog inputs from SKT1 to SKT8 to their respective input, B, D, F, H, J , L, N and P.

LK5 This link is put in place for applications that require data to be transmitted and received at the same time, i.e., it ties $\overline{TFS}$ and $\overline{RFS}$ together. If this facility is not required then the link is omitted.

Internal Clocking Mode

LK1 Both links in Position B configuring both SCLK and $\overline{RFS}$ as outputs.

All other links can be configured as for the external clocking mode described above.

CONTROLLING THE AD7890

There are two modes (external clocking and self-clocking) of operation applicable to the AD7890 and are selected by the SMODE pin which is controlled from LK1 on the evaluation board. Channel selection is controlled through a 5-bit control register which is accessible through the serial port (SKT14). This control register contains three bits for channel address, a software conversion start bit and a bit to put the part into sleep mode. There are two methods of initiating a conversion on the AD7890, the software conversion start and a hardware conversion start which can be applied through the conversion start input (SKT10). A rising edge on this $\overline{CONVST}$ input puts the track/hold into hold mode and a conversion is initiated. The conversion time for the part is determined from the clock signal applied to CLK IN (SKT11) on the board. With a 2.5 MHz master clock, conversion time for the AD7890 is 5.9 µs from the rising edge of the $\overline{CONVST}$ signal. 2 µs is required for track/hold acquisition time. An internal pulse is generated and appears on C_{EXT} whenever a multiplexer address is loaded to the AD7890 control register, and its duration will depend on the value of C_{EXT} used. In applications where the multiplexer is switched and conversion is initiated at the same time a 120 pF capacitor should be connected to C_{EXT} to allow for the acquisition time of the track/hold before conversion is initiated.

Software conversion starts are initiated by writing a logic 1 to the CONV bit of the control register. The internal pulse and the conversion process are initiated after the sixth serial clock cycle of the write cycle if a 1 is written to the CONV bit. With a 1 in the CONV bit the external $\overline{CONVST}$ input is disabled. Writing a 0 to the CONV bit in the control register enables the external convert start.

External Clocking Mode

The AD7890 is configured for its external clocking mode by tying the SMODE pin of the device to a logic high (LK1 on evaluation board in Position A). In this mode, SCLK and $\overline{RFS}$ of the AD7890 are configured as inputs. This external clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors. Figure 3 shows a timing and control sequence required to obtain optimum performance from the part in external clocking mode.

In the sequence shown in Figure 3, conversion is initiated on the rising edge of $\overline{CONVST}$, and new data is available in the output register of the AD7890 5.9 µs later. Once the read operation has taken place, a further 500 ns should be allowed before the next rising edge of $\overline{CONVST}$ to optimize the settling of the track/hold before the next conversion is initiated. The diagram shows the read operation and the write operation taking place in parallel. On the sixth falling edge of SCLK in the write sequence, the internal pulse will be initiated. Assuming MUX OUT is connected to SHA IN, 2 µs are required between this sixth falling edge of SCLK and the rising edge of $\overline{CONVST}$ to allow for the full acquisition time of the track/hold amplifier. With the serial clock rate at its maximum of 10 MHz, the achievable throughput rate for the part is 5.9 µs (conversion time) plus 0.6 µs (six serial clock pulses before internal pulse is initiated) plus 2 µs (acquisition time). This results in a minimum throughput time of 8.5 µs (equivalent to a throughput rate of 117 kHz). If the part is operated with a slower serial clock, it will impact the achievable throughput rate.

Applications that want to achieve optimum performance from the AD7890 will have to ensure that the data read does not occur during conversion or during 500 ns prior to the rising edge of $\overline{CONVST}$. This can be achieved in either of two ways. The first is to ensure in software that the read operation is not initiated until 5.9 µs after the rising edge of $\overline{CONVST}$. This will only be possible if the software knows when the $\overline{CONVST}$ command is issued. The second scheme would be to use the $\overline{CONVST}$ signal as both the conversion start signal and an interrupt signal. The simplest way to do this would be to generate a square wave signal for $\overline{CONVST}$ with high and low times of 5.9 µs (see Figure 4). Conversion is initiated on the rising edge of $\overline{CONVST}$. The falling edge of $\overline{CONVST}$ occurs 5.9 µs later and can be used as either an active low or falling edge-triggered interrupt signal to tell the

processor to read the data from the AD7890. Provided the read operation is completed 500 ns before the rising edge of $\overline{CONVST}$, the AD7890 will operate to specification. This scheme limits the throughput rate to 11.8 µs minimum.

Self-Clocking Mode

The AD7890 is configured for its self-clocking mode by tying the SMODE pin of the device to a logic low (LK1 on board in position B). In this mode, the AD7890 provides the serial clock signal and the serial data framing signal used for the transfer of data from the AD7890. This self-clocking mode can be used with processors that allow an external device to clock their serial port including most digital signal processors. Interface timing can be obtained from the AD7890 data sheet.

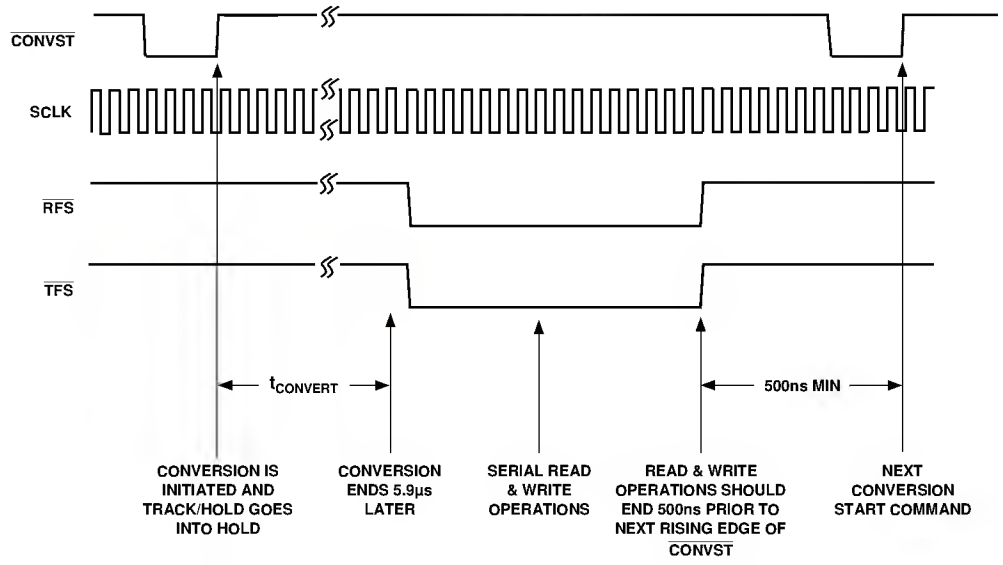

Figure 3. Control Sequence to Obtain Optimum Performance from the AD7890

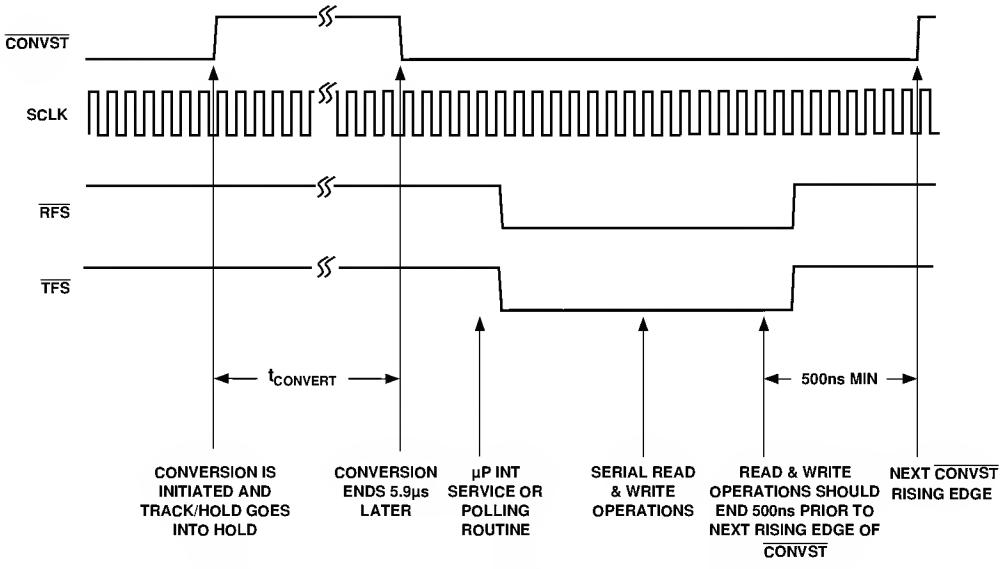

Figure 4. Sequence Using $\overline{CONVST}$ as an Interrupt Signal

COMPONENT LIST

Integrated Circuits

IC1	AD7890
IC3	AD780 Voltage Reference
IC4, IC5	AD713 Buffer Amplifier
IC6	LM78L05 Voltage Regulator
IC7	74HC4050 Hex Buffer
IC8	74HC125 Quad Bus Buffers with Three State Outputs

Capacitors

C2, C4, C6, C8, C10 C12, C14	10 µF Capacitors
C1, C3, C5, C7, C9 C11, C13, C15	0.1 µF Capacitors
C17, C18	0.1 µF Capacitors
C16	200 pF Capacitor

Resistors

R1, R2, R3, R4	10 kΩ Resistors

Links

LK1, LK2, LK3, LK4, LK5	Shorting Plugs

Sockets

SKT1 to SKT13	Subminiature BNC Sockets
SKT14	9-Way D Type Connector

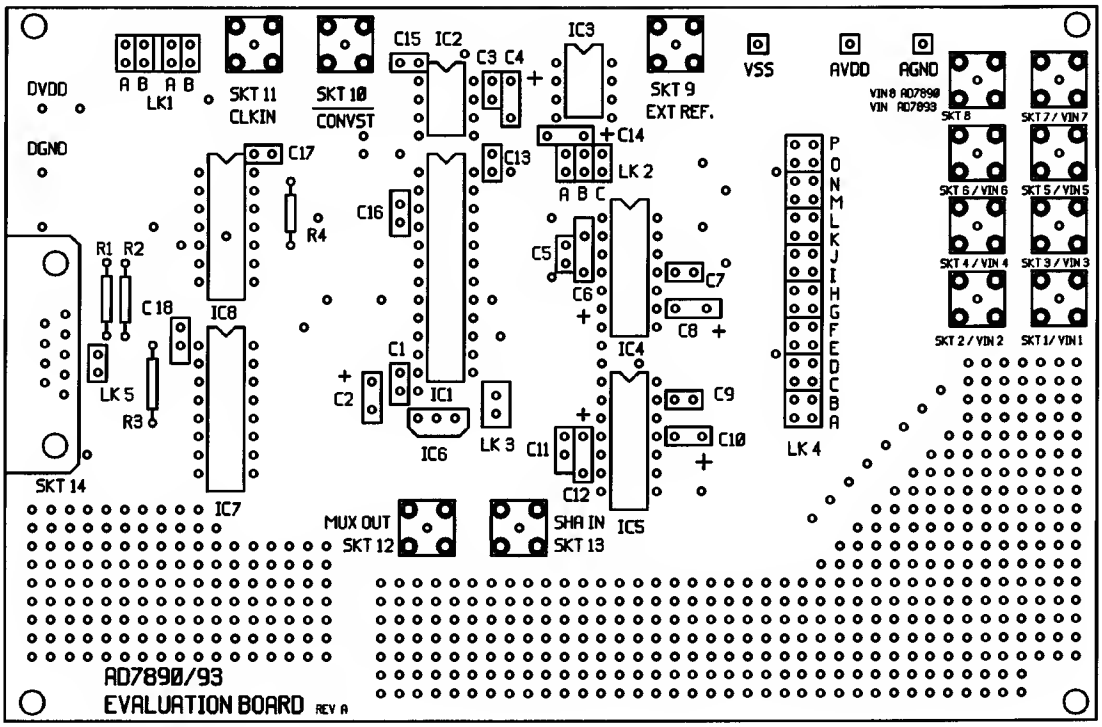

Figure 5. Silkscreen Layout for Evaluation Board

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